dLAN® Green PHY Module

Data sheet

DESCRIPTION

The dLAN® Green PHY Module is an integrated device for transmitting and receiving data over the power line. It holds all functions necessary for the easy creation of Green PHY network devices.

The QCA7000 Green PHY processor is supported by an LPC1758 host processor for additional interfaces and functionality.

Delivery status:

- The module supports Ethernet to PLC bridging functionality.
- It will automatically join a standard powerline network with default network password “HomePlugAV”. The network password may be changed by user interaction.

Customers are enabled to add or adapt functionality to their special needs by modifying the host processor firmware.

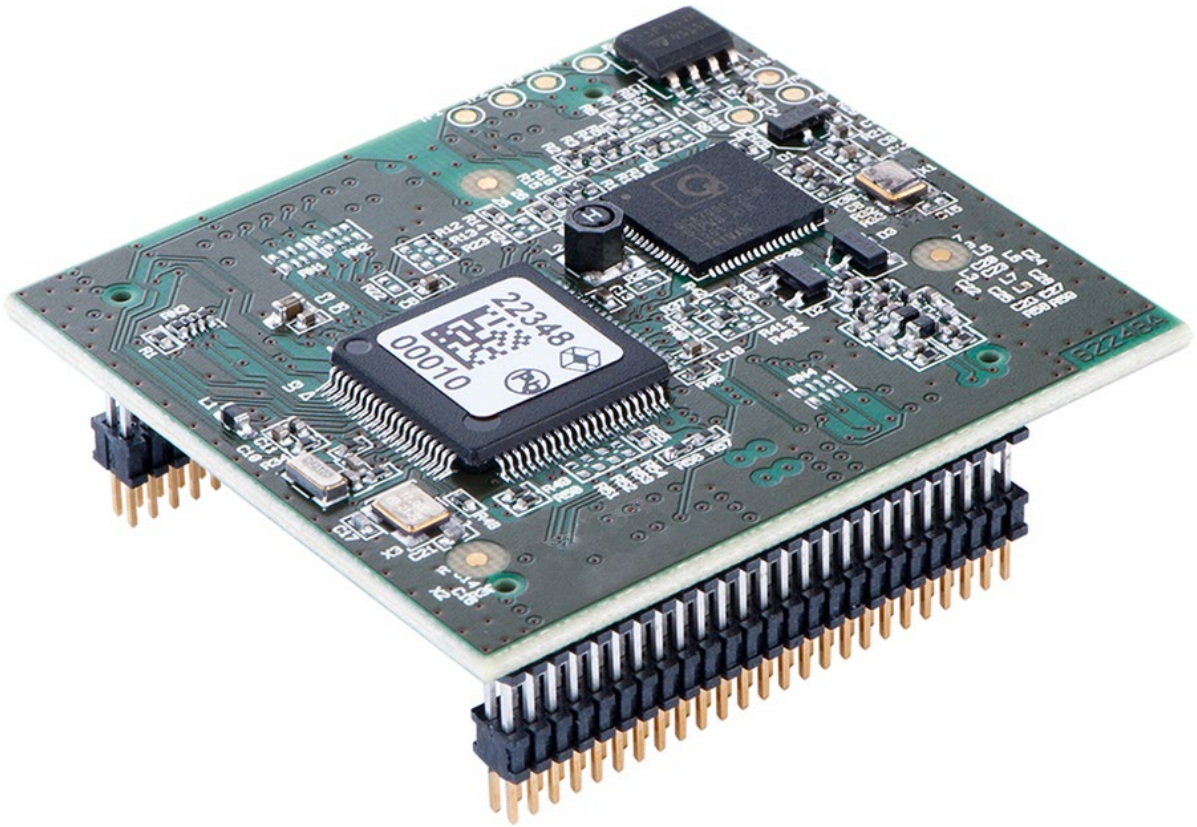
For further firmware related issues, please see Green PHY SDK (software development kit) documentation.

FEATURES

- Up to 10 Mbps data rate on the power line
- 600 m range via coaxial cable (preliminary)
- 400 m range via telephone line (prel.)
- 300 m range via power cable (prel.)
- Fully compatible with HomePlug Green PHY and HomePlug AV standards
- Open API for status information and device configuration
- 128 bit AES network encryption
- Fully integrated Green PHY power line networking controller with integrated UART/SPI interface
- QCA7000 chipset
- LPC1758 host processor
- Communication interfaces (multiplexed); connections available (implementation possible):
  - 4x UART (up to 1mbps)
  - SPI
  - Fast Ethernet
  - USB
  - CAN 2.0B
  - PWM / Motor control
  - 2x I²C
  - 12 bit ADC up to 200 kHz
  - 10 bit DAC
  - SSP
  - General purpose I/O
- 3.3 V single source operation voltage
- consumption < 1.5 W in smart meter scenario (1 kByte/s)
- Simplifies development cycle, assembly, testing, and certification approvals
- Physical dimensions: 39,4 mm x 43,2 mm x 16,09 mm (including pins)
- Designed for small-footprint applications

APPLICATIONS

- Charging control for e-mobility
- Home Automation
- Automated Meter Reading (AMR) / Smart Metering



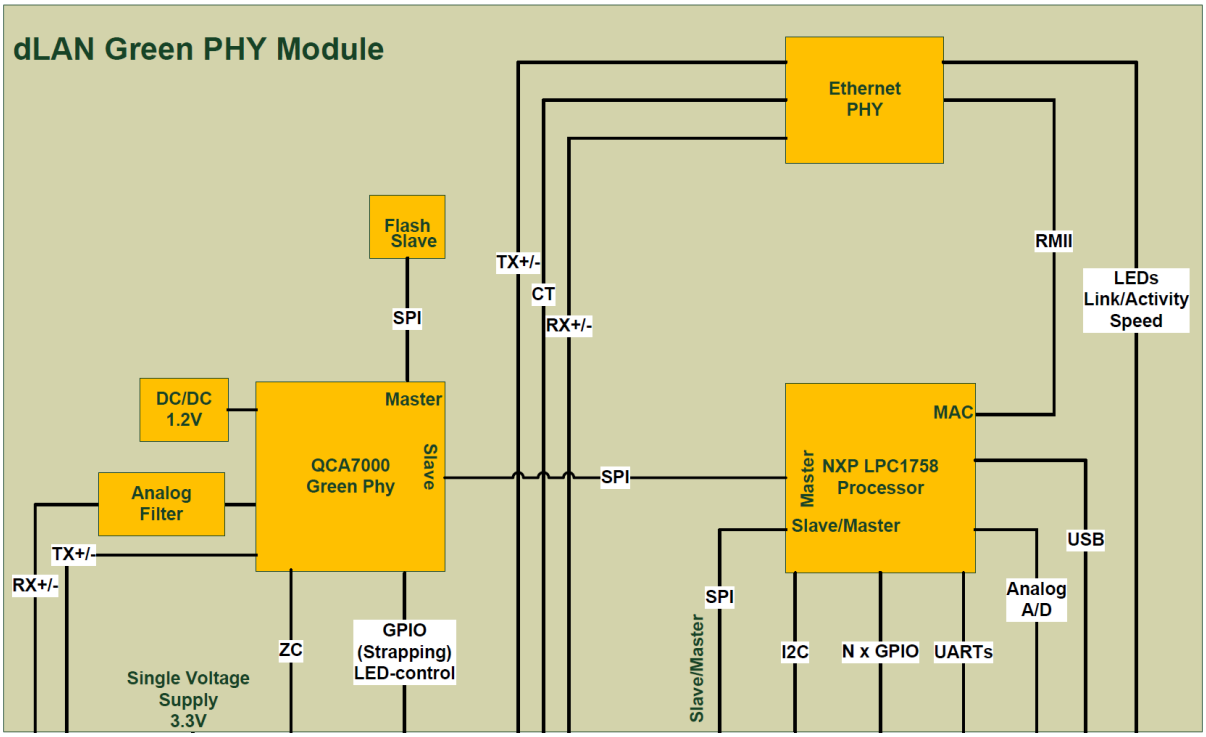


Fig. 1: Block Diagram of the devolo dLAN Green PHY Module

Contents

1 Integration of the dLAN® Green PHY Module into Existing Products

1.1 Pin multiplexing

All interfaces share a common set of pins to the mainboard. The individual functions are programmable depending on customer's needs. Multiplexed processor pins are routed 1:1 to module interface. Not all interface functions are available simultaneously.

2 Configuration of the dLAN® Green PHY Module

An external configuration is not necessary.

3 Security Pushbutton

The security pushbutton provides an easy method for pairing two or more dLAN devices. By pressing the pushbutton for a short period of time on each device that should be added to the network the devices are connected as if they had the same password.

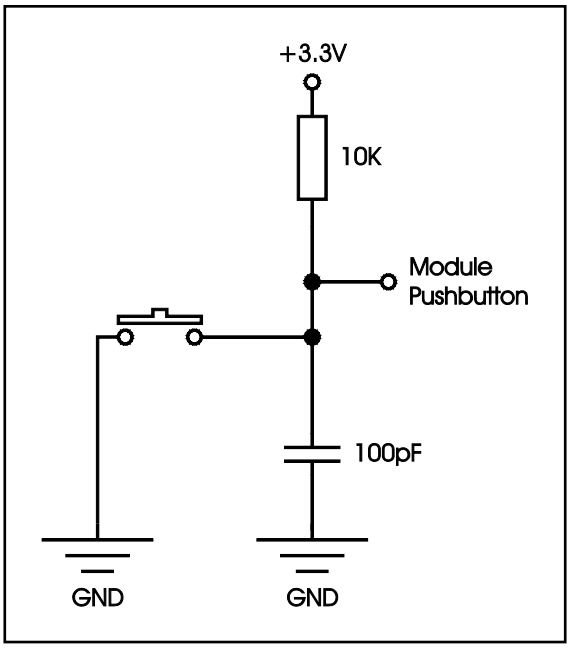


Fig. 2: Pushbutton circuitry

A schematic of the pushbutton circuitry appears in Fig. 2. When the pushbutton is pressed the pushbutton pin is pulled to ground (logical '0').

Default pushbutton timing:

0.1 sec < Tp < 3sec	Start pairing sequence
0.1 sec < Tp < 3sec	If in pairing sequence: terminate pairing sequence
10sec < Tp	Device is configured with random new network password

4 Green PHY GPIOs and Power On Configuration

The four Green PHY GPIO's (GPIO0–3) are used for system status indication and security pushbutton. All Green PHY GPIO's are used as boot strap configuration. Their state will be latched during the positive edge of the reset signal. You can connect a pushbutton according to Fig. 2 and LEDs according to Fig. 3. The maximum LED current should be limited to 12 mA.

Pin	QCA7000 Boot Strap Configuration	Pull-Up/Down on Module
GPIO0	High	PU
GPIO1	Low	PD
GPIO2	High	PU
GPIO3	High	PU

Table 1: Boot strapping configuration

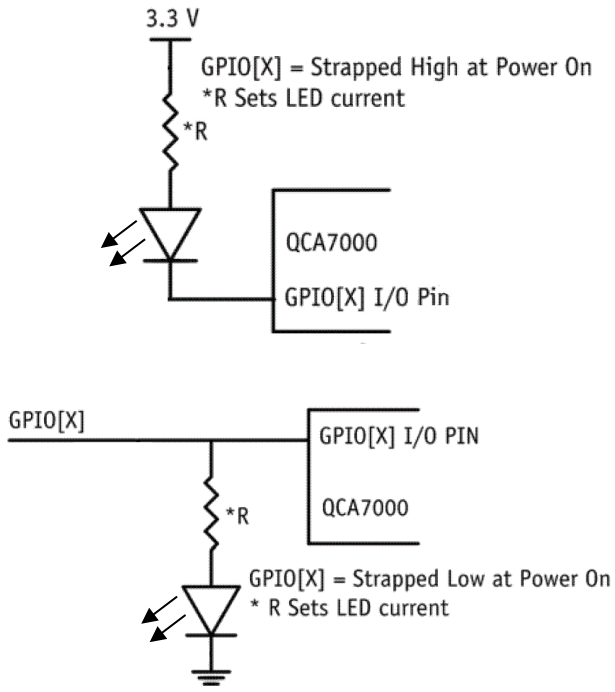


Fig. 3: LED strapping

5 Zero Cross

The Green PHY Module has an integrated analog Zero crossing detector included that detects when the 50 Hz or 60 Hz AC powerline voltage crosses through zero volts.

6 Application Examples

6.1 dLAN® Green PHY Module based HomePlug Device

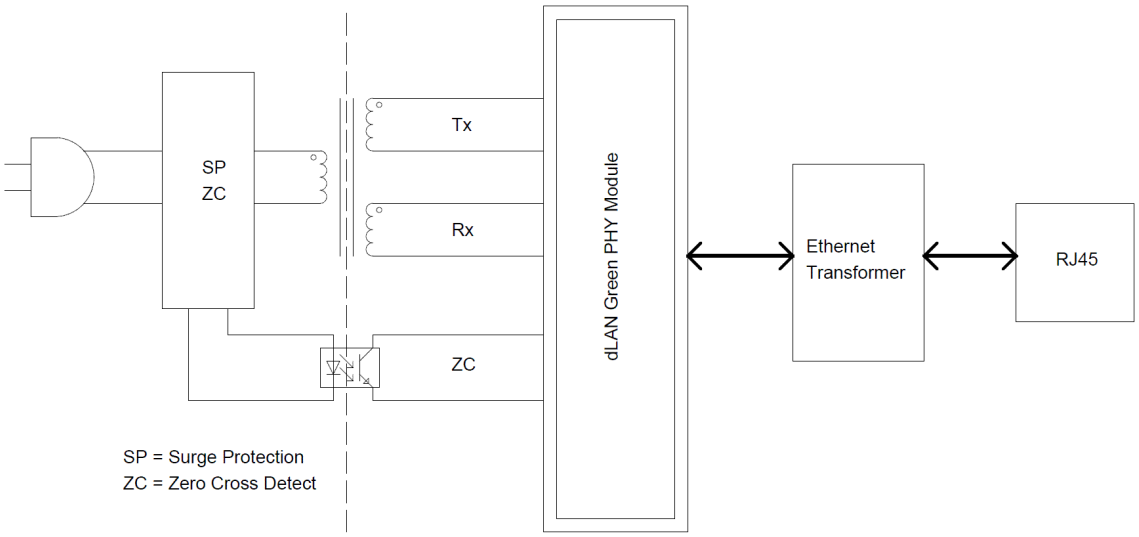


Fig. 4: dLAN Green PHY Module based HomePlug device

7 dLAN® Green PHY Module J1 Pinout

7.1 Pin Names

Pin No.	Pin Name	Type	Function
1	GND	P	**Ground:** 0 V reference
2	VDD	P	**3.3 V** supply voltage
3	P0[11] / RXD2 / SCL2 / MAT3[1]	I/O I I/O O	**P0[11] —** General purpose digital input/output pin. **RXD2 —** Receiver input for UART2. **SCL2 —** I2C2 clock input/output (this pin does not use a specialized I2C pad, see LPC17xx user manual Section 19.1 for details). **MAT3[1] —** Match output for Timer 3, channel 1.
4	P0[10] / TXD2 / SDA2 / MAT3[0]	I/O O I/O O	**P0[10] —** General purpose digital input/output pin. **TXD2 —** Transmitter output for UART2. **SDA2 —** I2C2 data input/output (this pin does not use a specialized I2C pad, see LPC17xx user manual Section 19.1 for details). **MAT3[0] —** Match output for Timer 3, channel 0.
5	P2[2] / PWM1[3] / CTS1 / TRACEDATA[3]	I/O O I O	**P2[2] —** General purpose digital input/output pin. **PWM1[3] —** Pulse Width Modulator 1, channel 3 output. **CTS1 —** Clear to Send input for UART1. **TRACEDATA[3] —** Trace data, bit 3.
6	P2[7] / RD2 / RTS1	I/O I O	**P2[7] —** General purpose digital input/output pin. **RD2 —** CAN2 receiver input. **RTS1 —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
7	P2[4] / PWM1[5] / DSR1 / TRACEDATA[1]	I/O O I O	**P2[4] —** General purpose digital input/output pin. **PWM1[5] —** Pulse Width Modulator 1, channel 5 output. **DSR1 —** Data Set Ready input for UART1. **TRACEDATA[1] —** Trace data, bit 1.
8	P2[5] / PWM1[6] / DTR1 / TRACEDATA[0]	I/O O O O	**P2[5] —** General purpose digital input/output pin. **PWM1[6] —** Pulse Width Modulator 1, channel 6 output. **DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal. **TRACEDATA[0] —** Trace data, bit 0.
9	P2[3] / PWM1[4] / DCD1 / TRACEDATA[2]	I/O O I O	**P2[3] —** General purpose digital input/output pin. **PWM1[4] —** Pulse Width Modulator 1, channel 4 output. **DCD1 —** Data Carrier Detect input for UART1. **TRACEDATA[2] —** Trace data, bit 2.
10	P2[6] / PCAP1[0] / RI1 / TRACECLK	I/O I I O	**P2[6] —** General purpose digital input/output pin. **PCAP1[0] —** Capture input for PWM1, channel 0. **RI1 —** Ring Indicator input for UART1. **TRACECLK —** Trace Clock.
11	P2[1] / PWM1[2] / RXD1	I/O O I	**P2[1] —** General purpose digital input/output pin. **PWM1[2] —** Pulse Width Modulator 1, channel 2 output. **RXD1 —** Receiver input for UART1.
12	P2[0] / PWM1[1] / TXD1	I/O O O	**P2[0] —** General purpose digital input/output pin. **PWM1[1] —** Pulse Width Modulator 1, channel 1 output. **TXD1 —** Transmitter output for UART1.

13	GND	P	**Ground:** 0 V reference
14	VDD	P	**3.3 V** supply voltage
15	GND	P	**Ground:** 0 V reference
16	P1[30] / V_{BUS} / AD0[4]	I/O I I	**P1[30] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **V_{BUS} —** Monitors the presence of USB bus power. Note: This signal must be HIGH for USB reset to occur. **AD0[4] —** A/D converter 0, input 4.
17	P1[19] / MCOA0 / nUSB_PPWR / CAP1[1]	I/O O O I	**P1[19] —** General purpose digital input/output pin. **MCOA0 —** Motor control PWM channel 0, output A. **nUSB_PPWR —** Port Power enable signal for USB port. **CAP1[1] —** Capture input for Timer 1, channel 1.
18	P1[22] / MCOB0 / USB_PWRD / MAT1[0]	I/O O I O	**P1[22] —** General purpose digital input/output pin. **MCOB0 —** Motor control PWM channel 0, output B. **USB_PWRD —** Power Status for USB port (host power switch). **MAT1[0] —** Match output for Timer 1, channel 0.
19	P2[9] / USB_CONNECT / RXD2	I/O O I	**P2[9] —** General purpose digital input/output pin. **USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. **RXD2 —** Receiver input for UART2.
20	P0[30] / USB_D−	I/O I/O	**P0[30] —** General purpose digital input/output pin. Pad provides digital I/O and USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). **USB_D− —** USB bidirectional D− line. A 33 Ohm resistor in series is integrated on Module.
21	P1[18] / USB_UP_LED / PWM1[1] / CAP1[0]	I/O O O I	**P1[18] —** General purpose digital input/output pin. **USB_UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend. **PWM1[1] —** Pulse Width Modulator 1, channel 1 output. **CAP1[0] —** Capture input for Timer 1, channel 0.
22	P0[29] / USB_D+	I/O I/O	**P0[29] —** General purpose digital input/output pin. Pad provides digital I/O and USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). **USB_D+ —** USB bidirectional D+ line. A 33 Ohm resistor in series is integrated on Module.
23	GND	P	**Ground:** 0 V reference
24	VDD	P	**3.3 V** supply voltage
25	P1[25] / MCOA1 / MAT1[1]	I/O O O	**P1[25] —** General purpose digital input/output pin. **MCOA1 —** Motor control PWM channel 1, output A. **MAT1[1] —** Match output for Timer 1, channel 1.
26	RSVD		Reserved, do not connect.
27	RSVD		Reserved, do not connect.
28	RSVD		Reserved, do not connect.
29	RSVD		Reserved, do not connect.
30	RSVD		Reserved, do not connect.
31	RSVD		Reserved, do not connect.
32	RSVD		Reserved, do not connect.

33	RSVD		Reserved, do not connect.
34	RSVD		Reserved, do not connect.
35	RSVD		Reserved, do not connect.
36	RSVD		Reserved, do not connect.
37	GND	P	**Ground:** 0 V reference
38	VDD	P	**3.3 V** supply voltage
39	P0[26] / AD0[3] / AOUT / RXD3	I/O I O I	**P0[26] —** General purpose digital input/output pin. When configured as an ADC input or DAC output, the digital section of the pad is disabled. **AD0[3] —** A/D converter 0, input 3. **AOUT —** D/A converter output. **RXD3 —** Receiver input for UART3.
40	P1[31] / SCK1 / AD0[5]	I/O I/O I	**P1[31] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **SCK1 —** Serial Clock for SSP1. **AD0[5] —** A/D converter 0, input 5.
41	GND	P	**Ground:** 0 V reference
42	P0[25] / AD0[2] / I2SRX_SDA / TXD3	I/O I I/O O	**P0[25] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **AD0[2] —** A/D converter 0, input 2. **I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S bus specification*. **TXD3 —** Transmitter output for UART3.
43	TDI	I	**TDI —** Test Data in for JTAG interface.
44	VDD	P	**3.3 V** supply voltage
45	TMS / SWDIO	I I/O	**TMS —** Test Mode Select for JTAG interface. **SWDIO —** Serial wire debug data input/output.
46	TDO / SWO	O O	**TDO —** Test Data out for JTAG interface. **SWO —** Serial wire trace output.
47	TCK / SWDCLK	I I	**TCK —** Test Clock for JTAG interface. **SWDCLK —** Serial wire clock.
48	nTRST	I	**nTRST —** Test **Reset** for JTAG interface.
49	GND	P	**Ground:** 0 V reference
50	VDD	P	**3.3 V** supply voltage

Table 2: dLAN Green PHY Module J1 pin description

8 dLAN® Green PHY Module J2 Pinout

8.1 Pin Names

Pin No.	Pin Name	Type	Function
1	GND	P	**Ground:** 0 V reference
2	GND	P	**Ground:** 0 V reference
3	G-PHY_ RXP	I	**RXP —** PLC Positive differential input.
4	G-PHY _TXP	O	**TXP** — PLC Positive differential output.
5	G-PHY _RXN	I	**RXN —** PLC Negative differential input.
6	G-PHY _TXN	O	**TXN —** PLC Negative differential output.
7	GND	P	**Ground:** 0 V reference
8	GND	P	**Ground:** 0 V reference
9	G-PHY_ZC_IN	I	**ZC_IN —** Zero Cross Input
10	RSVD		Reserved, do not connect.
11	G-PHY _GPIO[0]	I/O	**GPIO 0 —** Sets mode at power on, then becomes I/O.
12	G-PHY _GPIO[1]	I/O	**GPIO 1 —** Sets mode at power on, then becomes I/O.
13	G-PHY _GPIO[2]	I/O	**GPIO 2 —** Sets mode at power on, then becomes I/O.
14	G-PHY _GPIO[3]	I/O	**GPIO 3 —** Sets mode at power on, then becomes I/O.
15	RSVD		Reserved, do not connect.
16	RSVD		Reserved, do not connect.
17	RSVD		Reserved, do not connect.
18	RSVD		Reserved, do not connect.
19	VDD	P	**3.3 V** supply voltage
20	RSVD		Reserved, do not connect.
21	VDD	P	**3.3 V** supply voltage
22	GND	P	**Ground:** 0 V reference
23	ETH_TXP	I/O	**TXP** – Ethernet Transmit/Receive Positive Channel 1.
24	ETH_RXP	I/O	**RXP** – Ethernet Transmit/Receive Positive Channel 2.
25	ETH_TXN	I/O	**TXN** – Ethernet Transmit/Receive Negative Channel 1.
26	ETH_RXN	I/O	**RXN** – Ethernet Transmit/Receive Negative Channel 2.
27	ETH_VDDCTx	O	**VDDCTx** – Ethernet XFMR CTx (Common Tap) Power supply.
28	ETH_VDDCTX	O	**VDDCTx** – Ethernet XFMR CTx (Common Tap) Power supply.
29	VDD	P	**3.3 V** supply voltage
30	GND	P	**Ground:** 0 V reference
31	ETH_LED1	O	**LED1** – Sets mode at power on then becomes Ethernet Link/Activity LED indication (active High).
32	ETH_LED2	O	**LED2** – Sets mode at power on then becomes Ethernet Link Speed LED indication (active Low). 100 = on, 10 = off.

33	P2[10] / nEINT0 / NMI	I/O I I	**P2[10] —** General purpose digital input/output pin. 5 V tolerant pad with 5ns glitch filter providing digital I/O functions with TTL levels and hysteresis. **Note:** A LOW on this pin while RESET is LOW forces the on-chip bootloader to take over control of the part after a reset and go into ISP mode. See LPC17xx user manual Section 32.1 for details. **nEINT0 —** External interrupt 0 input. **NMI —** Non-maskable interrupt input.
34	RSVD		Reserved, do not connect.
35	P0[2] / TXD0 / AD0[7]	I/O O I	**P0[2] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **TXD0 —** Transmitter output for UART0. **AD0[7] —** A/D converter 0, input 7.
36	P0[3] / RXD0 / AD0[6]	I/O I I	**P0[3] —** General purpose digital input/output pin. When configured as an ADC input, digital section of the pad is disabled. **RXD0 —** Receiver input for UART0. **AD0[6] —** A/D converter 0, input 6.
37	P0[8] / I2STX_WS / MISO1 / MAT2[2]	I/O I/O I/O O	**P0[8] —** General purpose digital input/output pin. **I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I2S bus specification*. **MISO1 —** Master In Slave Out for SSP1. **MAT2[2] —** Match output for Timer 2, channel 2.
38	P0[9] / I2STX_SDA / MOSI1 / MAT2[3]	I/O I/O I/O O	**P0[9] —** General purpose digital input/output pin. **I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I2S bus specification*. **MOSI1 —** Master Out Slave In for SSP1. **MAT2[3] —** Match output for Timer 2, channel 3.
39	P0[6] / I2SRX_SDA / SSEL1 / MAT2[0]	I/O I/O I/O O	**P0[6] —** General purpose digital input/output pin. **I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I2S bus specification*. **SSEL1 —** Slave Select for SSP1. **MAT2[0] —** Match output for Timer 2, channel 0.
40	P0[7] / I2STX_CLK / SCK1 / MAT2[1]	I/O I/O I/O O	**P0[7] —** General purpose digital input/output pin. **I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I2S bus specification*. **SCK1 —** Serial Clock for SSP1. **MAT2[1] —** Match output for Timer 2, channel 1.
41	P0[0] / RD1 / TXD3 / SDA1	I/O I O I/O	**P0[0] —** General purpose digital input/output pin. **RD1 —** CAN1 receiver input. **TXD3 —** Transmitter output for UART3. **SDA1 —** I2C1 data input/output (this pin does not use a specialized I2C pad, see LPC17xx user manual Section 19.1 for details).
42	P0[1] / TD1 / RXD3 / SCL1	I/O O I I/O	**P0[1] —** General purpose digital input/output pin. **TD1 —** CAN1 transmitter output. **RXD3 —** Receiver input for UART3. **SCL1 —** I2C1 clock input/output (this pin does not use a specialized I2C pad, see LPC17xx user manual Section 19.1 for details).
43	VBAT	P	**VBAT —** RTC power supply: Typically connected to an external 3V battery. If this pin is not powered, the RTC is still powered internally if VDD is present.
44	RSVD		Reserved, do not connect.

45	P1[26] / MCOB1 / PWM1[6] / CAP0[0]	I/O O O I	**P1[26] —** General purpose digital input/output pin. **MCOB1 —** Motor control PWM channel 1, output B. **PWM1[6] —** Pulse Width Modulator 1, channel 6 output. **CAP0[0] —** Capture input for Timer 0, channel 0.
46	P1[28] / MCOA2 / PCAP1[0] / MAT0[0]	I/O O I O	**P1[28] —** General purpose digital input/output pin. **MCOA2 —** Motor control PWM channel 2, output A. **PCAP1[0] —** Capture input for PWM1, channel 0. **MAT0[0] —** Match output for Timer 0, channel 0.
47	nRSTOUT	O	**nRSTOUT —** This is a 3.3 V pin. A LOW output on this pin indicates that the device is in the reset state, for any reason. This reflects the RESET input pin and all internal reset sources.
48	nRESET	I	**nRESET —** External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This is a 5 V tolerant pad with a 20 ns glitch filter, TTL levels and hysteresis.
49	VDD	P	**3.3 V** supply voltage
50	GND	P	**Ground:** 0 V reference

Table 3: dLAN® Green PHY Module J2 pin description

9 dLAN® Green PHY Module Specifications

9.1 Power Supply Requirements

The dLAN® Green PHY Module needs a 3.3V single source for operation.

Symbol	Parameter	Min	Typ	Max
V_{DD}	Power Supply Voltage	3.15 V	3.3 V	3.45 V
P	Power		1.5W	2.5W

Table 4: Power supply requirements

9.2 Reset Signal Requirements

The reset signal has to be driven low for at least 100 ms after all supply voltages are stable.

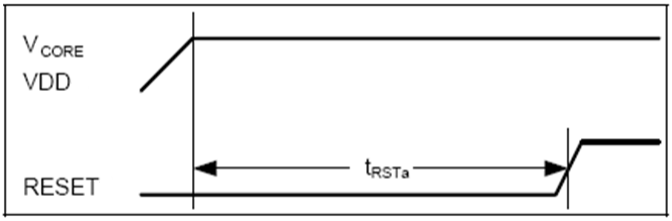


Fig. 5: Reset timing – t_{RSTa} = 100 ms min.

9.3 Absolute Maximum Ratings

Operation at or above the absolute maximum ratings may cause permanent damage to the device. Exposure to these conditions for extended periods of time may affect long-term device reliability. Correct functional behaviour is not implied or guaranteed when operating at or above the absolute maximum ratings.

Symbol	Parameter	Min	Max
V_{DD}	Power Supply Voltage	-0.3 V	3.6 V
Digital	Digital lines	Vss-0.3 V	V_{DD}+0.3 V
Analog	Analog lines	Vss-0.3 V	V_{DD}+0.3 V
T_{STORE}	Storage Temperature	-40°C	150°C
$T_{OPERATE}$	Operation Temperature	-25°C	70°C
V_{ESD}	Electrostatic Discharge		2000 V

Table 5: Absolute maximum ratings

The power consumption depends on additional implemented functionality;
a maximum power consumption of 2.5W may be assumed.

9.4 DC Characteristics

Parameter	Test Conditions	Min	Max
Low-level input voltage			0.8 V
High-level input voltage		2.0V	
Low-level output voltage	I_{OL}=4mA, 12mA[1]		0.4 V
High-level output voltage	I_{OH}=-4mA, -12mA[2]	2.4V	
Low-level input current	V_I=GND	-1µA	
High-level input current	V_I=VDD		1µA
High-impedance output current	GND ≤ V_I ≤ VDD	-1µA	1µA

Table 6: DC characteristics

1) I_{OL}= 12mA for status LEDs
   I_{OL}= 4mA for all other interfaces
2) I_{OH}= -12mA for status LEDs
   I_{OH}= -4mA for all other interfaces

9.5 Mechanical Specifications

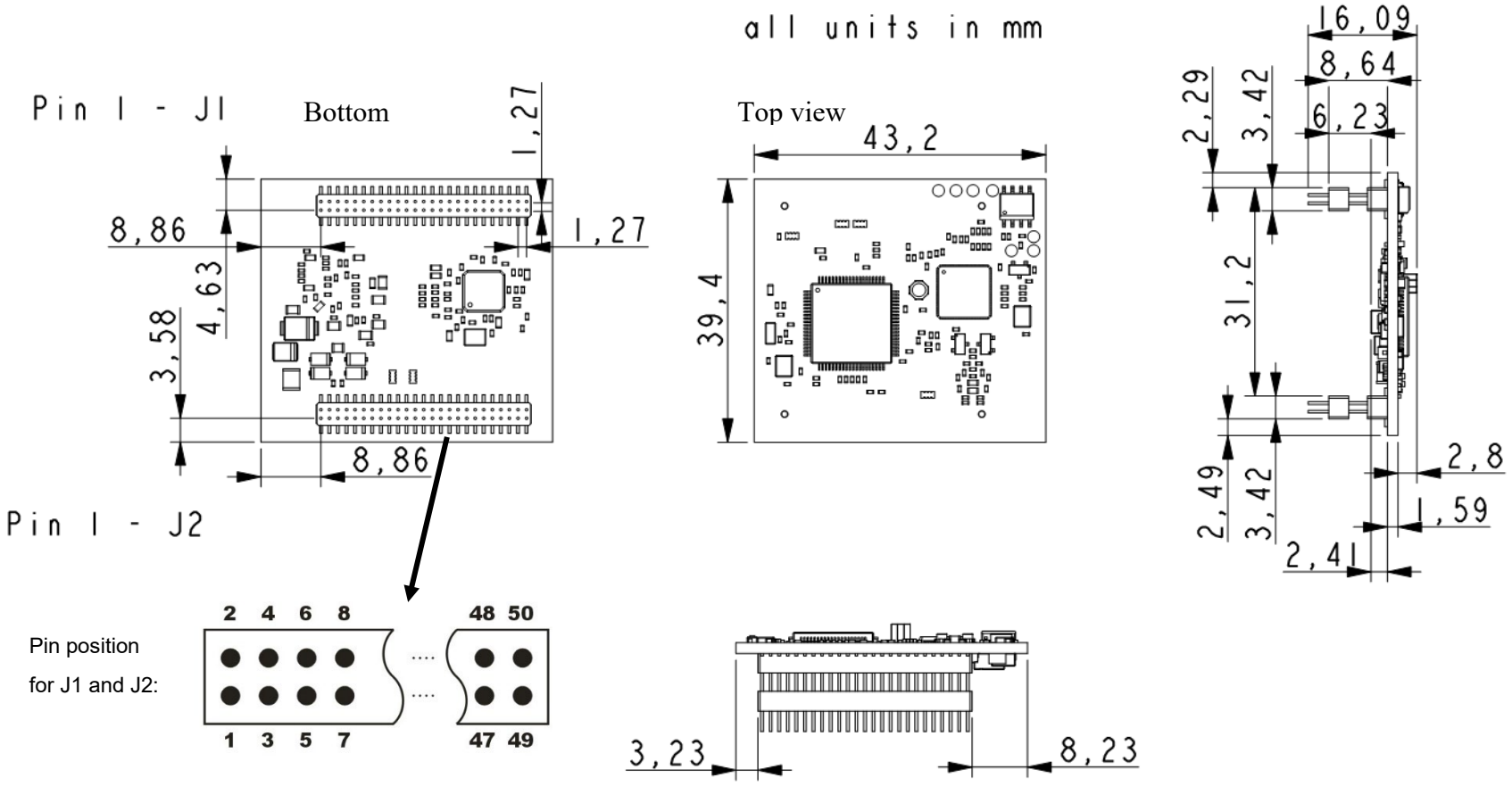


Fig. 6: dLAN® Green PHY Module dimensions

- Connector type J1 and J2 (Header male 2x25 1.27mm SMD):
- Successful, PCM220-50G002-T (or similar)
  -> click PCM220-50G002-T and find the fie in the download area
- Recommended counterpart connector (Header female 2x25 1.27mm SMD):
- Successful, FCM244-50G05-P1 (or similar)
  -> click FCM244-50G05-P1 and find the file in the download area

Mated height when using the recommended connectors:

➔ **13.2mm**

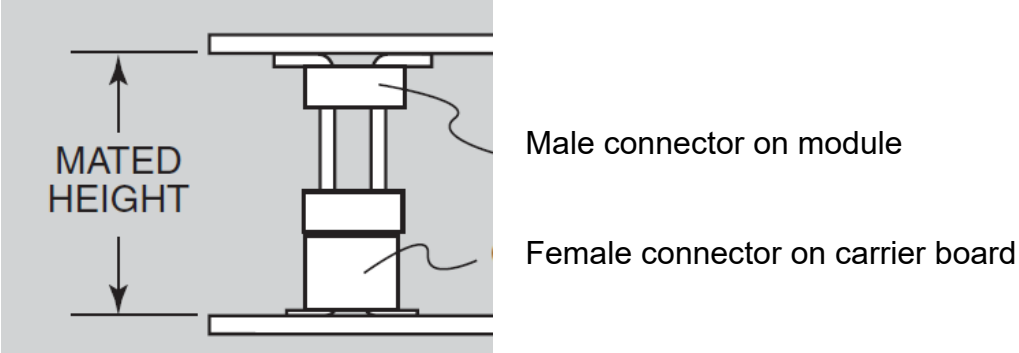


Fig. 7: dLAN® Green PHY Module mated height

10 LPC 1758 host processor

The LPC1758 host processor is used for

- SPI (SSP0 Interface) to Ethernet bridging functionality (default implementation).
  So the SSP0 interface – that is present on the module connector – cannot be used for further purposes!
- Realization of additional interfaces and integration of applications.

10.1 Specifications

- NXP LPC1758 Cortex-M3 processor
- 512 kB flash memory
- 64 kB SRAM
- Internal clock 100 MHz

10.2 Firmware and programming

The LPC1758 is running FreeRTOS at delivery.

Advise: For firmware update of the LPC, one of the following interfaces should be made accessible:

➔ JTAG

➔ UART0

See LPC17xx user manual “Chapter 32: LPC17xx Flash memory interface and programming” and devolo application note for details.

10.3 Additional information

Information about the LPC1758 can be obtained from the NXP website at:
LPC1758FBD80|Arm Cortex-M3|32-bit MCU | NXP Semiconductors
A data sheet is available at:
LPC1759_58_56_54_52_51 Product data sheet (nxp.com)

11 Revision History

Revision	Modifications
1	• Original Issue
1.1	• Added connector references
1.2	• Added block diagram
1.3	• Block diagram modified, LPC1758 info added
1.4	• Feature list improved
1.5	• First complete version • Pins J2-34 and J2-44 changed to reserved
1.6	• Minor explaining comments
1.7	• Temperature range extended from 55°C to 70°C
1.8	• Adaptation of Connector reference
1.9	• Changed links to NXP websites
1.10	• Temperature range extended from -25°C to -40°C
1.11	• Update Links to external Datasheets